

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Luiz Andre Barroso et al.

Confirmation No.:

Application No.:

Examiner: Li, Z.

Filing Date: Herewith

Group Art Unit: 2186

Title: METHOD AND SYSTEM FOR EXCLUSIVE TWO-LEVEL CACHING IN A CHIP-MULTIPROCESSOR

Commissioner for Patents

PO Box 1450

Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is submitted:

- (X) under 37 CFR 1.97(b), or
(Within three months of filing national application; or date of entry of national application; or before mailing date of first office action on the merits; whichever occurs last)
- () under 37 CFR 1.97(c) together with either a:
() Statement under 37 CFR 1.97(e), or
() a \$180.00 fee under 37 CFR 1.17(p), or
(After the CFR 1.97 (b) time period, but before final action or notice of allowance, whichever occurs first)
- () under 37 CFR 1.97 (d) together with a:
() Statement under 37 CFR 1.97(e)(1) or (2), and
() a \$180.00 fee set forth in 37 CFR 1.17(p).
(Filed after final action, a notice of allowance, on or before payment of the issue fee)

Please charge to Deposit Account 08-2025 the sum of \$0.00. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account 08-2025 pursuant to 37 CFR 1.25.

(X) Applicant(s) submit herewith Form PTO 1449 - Information Disclosure Statement together with any required copies of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

() A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Form 1449, as presently understood by the individual(s) designated in 37 CFR 1.56 (c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed on form PTO 1449 and is enclosed herewith.

It is requested that the information disclosed herein be made of record in this application.

"Express Mail" label no. EV 365 157 544 US

Respectfully submitted,

Date of Deposit 02-02-2004

Luz Andre Barroso et al.

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: Commissioner for Patents, Alexandria, VA 22313-1450.

By Helen Tinsley
Typed Name: Helen Tinsley

By Brent R. Knight

Brent R. Knight

Attorney/Agent for Applicant(s)
Reg. No. 54,226

Date: 02-02-2004

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LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT		APPLICANT Luiz Andre Barroso et al.		
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1Q	Agrawal, Anant, et al., "An Evaluation of Directory Schemes for Cache Coherence", Proceedings of 15th International Symposium on Computer Architecture ("ISCA") (May 1998) pp. 280-289
1R	Barroso, Luiz Andre, et al., "Impact of Chip-Level Integration on Performance of OLTP Workloads", High-Performance Computer Architecture ("HPCA") (January 2000)
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2Q	Eggers, Susan J., et al., "Simulation Multithreading: A Platform for Next-generation Processors", University of Washington, DEC Western Research Laboratory ((eggers.levyjlo)@cs.washington.edu) ((emer.stamm)@vssad.enet.dec.com) pp. 1-15 (1997)
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3Q	Hammond, Lance, et al., "A Single-Chip Multiprocessor", IEEE (September 1997) (0018-9162)
3R	Hammond, Lance, et al., "Data Speculation Support for a Chip Multiprocessor", Stanford University, Computer Systems Laboratory (http://www.hydra.stanford.edu/), (October 1998)
3S	Jouppi, Norman P., et al., "Tradeoffs in Two-Level On-Chip Caching", WRL Research Report 93/3, Western Research Laboratory (WRL-Techreports@decwri.dec.com) (December 1993) pp. 1-31

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4Q	Krishnan, Venkata, et al., "Hardware and Software Support for Speculative Execution of Sequential Binaries on a Chip-Multiprocessor", University of Illinois at Urbana-Champaign (http://iacoma.cs.uiuc.edu) (1998)
4R	Kuskin, Jeffrey, et al., "The Stanford FLASH Multiprocessor", Stanford University, Computer Systems Laboratory (June 6, 1996)
4S	Laudon, James, et al., "The SGI Origin: A ccNUMA Highly Scalable Server", Silicon Graphics, Inc. (laudon@sgi.com) (June 1997)

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5Q	Lenoski, Daniel et al., "The Directory-Based Cache Coherence Protocol for the DASH Multiprocessor", IEEE (1990) (CH2887-8) pp. 148-159
5R	Nayfeh, Basem A., et al., "Evaluation of Design Alternatives for a Multiprocessor Microprocessor", ACM (1996) (0-89791-786-3) pp. 67-77
5S	Nowatzky, Andreas G., et al., "S-Connect: from Networks of Workstations to Supercomputer Performance", 22nd Annual International Symposium on Computer Architecture ("ISCA") (June 1995)

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6Q	Nowatzky, Andreas, et al., "Exploiting Parallelism in Cache Coherency Protocol Engines", Sun Microsystems Computer Corporation (August 1995)
6R	Olukotun, Kunle, et al., "The Case of a Single-Chip Multiprocessor", Proceedings Seventh International Symposium Architectural Support for Programming Languages and Operating Systems ("ASPLOS VII") (October 1996)
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7R	Kunkel, Steven, et al., "System Optimization for OLTP Workloads, IEEE (1999) (0272-1732) pp. 56-64
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